§103 Rejection of the Claims

The Examiner has cited several combinations of references with respect to various combinations of claims. Specifically, the Examiner has cited Aronowitz, Selvakumar, Crabbe, Grider, and Wolf. Applicant respectfully asserts that the following arguments in combination with the amendments to the claims listed above, overcome the 35 USC § 103 rejections and place the claims in condition for allowance. The cited references are discussed below, both individually, and in combination, and Applicant's invention is distinguished from all references both individually and in combination.

Aronowitz appears to show a transistor containing a germanium rich layer 18. However, the germanium rich layer of Aronowitz has a molar fraction of 0.95 (col. 2, ln. 29-30). Aronowitz further discusses this limitation at col. 4, ln. 23-28, where it is stated that "the germanium-rich layer should be at least 95%." Aronowitz does not show or suggest a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction x, located underneath the SiO_2 gate oxide and between the source/drain regions, **wherein x is less than or equal to 0.6**, and wherein the $Si_{1-x}Ge_x$ channel region forms a $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

Selvakumar appears to show a transistor containing a SiGe channel region 8. However, Selvakumar teaches a "small SiGe region surrounded by silicon" (col. 4, ln. 17-20). While it appears that the "channel region" of Selvakumar creates an interface with a SiO_2 gate oxide, Selvakumar explicitly states that the SiGe element of the channel region is "surrounded by silicon all around" (Col. 5, ln. 33-36). The SiGe region of Selvakumar therefore is adjoined to a silicon region which in turn is adjoined to a SiO_2 gate oxide. Selvakumar does not show a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction x, located underneath the SiO_2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and **wherein the $Si_{1-x}Ge_x$ channel region forms a $Si_{1-x}Ge_x/SiO_2$ gate oxide interface**.

Crabbe appears to show a transistor containing a silicon germanium channel 18. However, the silicon germanium layer in Crabbe is "sandwiched between layers of pure silicon" (Col. 4, ln. 45-48). As further discussed in col. 6, ln. 22-28, a silicon cap layer 20 is deposited on the SiGe channel layer 18, and a gate insulator layer 22 is formed on the cap layer 20. Crabbe does not show or suggest a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction x, located underneath the SiO_2 gate oxide and between the source/drain regions, wherein x is less

than or equal to 0.6, and **wherein the $Si_{1-x}Ge_x$ channel region forms a $Si_{1-x}Ge_x/SiO_2$ gate oxide interface**.

Grider appears to show a transistor that contains a SiGe alloy layer 24. However, the Grider reference is directed towards solving a problem of forming contacts on shallow source/drain regions (col. 1, ln. 50-65). The SiGe layer in Grider is used at an interface between source/drain regions of a transistor to promote preferential polysilicon growth in these areas (col. 3, ln. 60-65). Grider does not show or suggest the use of SiGe in a channel region of the transistor. More specifically, Grider does not show or suggest a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction x, located underneath the SiO_2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

Wolf appears to discuss MOSFET transistors with small channel regions. Applicant assumes that Wolf was cited by the Examiner to support Examiner's argument concerning obviousness of channel lengths of a certain dimension. As amended, Applicant's claims do not include any limitations with respect to a channel dimension. Wolf does not show or suggest a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction x, located underneath the SiO_2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

In contrast, all independent claims of Applicant's invention as amended now include a **$Si_{1-x}Ge_x$ channel region, having a germanium molar fraction x, located underneath the SiO_2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a $Si_{1-x}Ge_x/SiO_2$ gate oxide interface**. Applicant notes the importance of the specified molar fraction range is discussed in the specification page 6 and in figure 2. Applicant also notes the importance of Applicant's novel implantation process through the gate oxide that allows the formation of a device including a $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

Because the listed references cited by the Examiner, alone or in combination, do not show or suggest the $Si_{1-x}Ge_x$ channel region described in bold above, a 35 USC § 103 is inappropriate. Withdrawal of Examiner's § 103 rejection with respect to independent claims 11, 24, 25, 28, 38, 40, and 41 is therefore respectfully requested. Dependent claims 32 and 39 have been amended

for agreement of terms with the claims they depend from. Because Applicant respectfully asserts that all independent claims are now in condition for allowance, withdrawal of Examiner's § 103 rejection with respect to dependent claims 13-14, 26-27, 32, 39, and 42-43 is also respectfully requested as they are dependent upon allowable claims.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6944 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box AF, Commissioner of Patents, Washington, D.C. 20231, on this 22 day of December, 2000.

Tina Ryan
Name

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